Orchestrating a brighter world

NEC creates the social values of safety, security, fairness and efficiency to promote a more sustainable world where everyone has the chance to reach their full potential.
Agenda

- SX-Aurora TSUBASA updates
- Studies for the future VE
SX-Aurora TSUBASA updates
SX-Aurora TSUBASA is the latest model of SX Vector computer series

<table>
<thead>
<tr>
<th>Model</th>
<th>SX-1/2</th>
<th>SX-3</th>
<th>SX-4</th>
<th>SX-5</th>
<th>SX-6</th>
<th>SX-7</th>
<th>SX-8/8R</th>
<th>SX-9</th>
<th>SX-ACE</th>
<th>SX-Aurora TSUBASA</th>
<th>SX-Aurora TSUBASA Gen2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>Bipolar</td>
<td>Bipolar</td>
<td>350 nm</td>
<td>250 nm</td>
<td>150 nm</td>
<td>150 nm</td>
<td>90 nm</td>
<td>65 nm</td>
<td>28 nm</td>
<td>16 nm</td>
<td>16 nm</td>
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<tr>
<td>CPU frequency</td>
<td>166 MHz</td>
<td>340 MHz</td>
<td>125 MHz</td>
<td>250 MHz</td>
<td>500 MHz</td>
<td>552 MHz</td>
<td>1.0 GHz</td>
<td>3.2 GHz</td>
<td>1.0 GHz</td>
<td>~1.6 GHz</td>
<td>~1.6 GHz</td>
</tr>
<tr>
<td>CPU performance</td>
<td>1.3 GF</td>
<td>5.5 GF</td>
<td>2.0 GF</td>
<td>8.0 GF</td>
<td>8.0 GF</td>
<td>8.8 GF</td>
<td>16.0 GF</td>
<td>102.4 GF</td>
<td>256.0 GF</td>
<td>~2.45 TF</td>
<td>~3.07 TF</td>
</tr>
<tr>
<td>CPU Memory bandwidth</td>
<td>10.7 GB/s</td>
<td>12.8 GB/s</td>
<td>16.0 GB/s</td>
<td>64.0 GB/s</td>
<td>32.0 GB/s</td>
<td>35.3 GB/s</td>
<td>64.0 GB/s</td>
<td>256.0 GB/s</td>
<td>256.0 GB/s</td>
<td>~1.22TB/s</td>
<td>~1.53TB/s</td>
</tr>
</tbody>
</table>
Architecture

- SX-Aurora TSUBASA = VH + VE
- Linux + standard language (Fortran/C/C++)
- Enjoy high performance with easy programming

**Software**
- Linux OS
- Fortran/C/C++ → No special programming like CUDA
- Automatic vectorization compiler

**Interconnect**
- InfiniBand for MPI
- VE-VE direct communication support

**Hardware**
- VH(Standard x86 server) + Vector Engine

**Easy programming** (standard language) ➔ **Automatic vectorization compiler** ➔ **Enjoy high Performance!**

Linux OS

x86 server (VH)

Vector Engine (VE)

PCIe

Application

Orchestrating a brighter world

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Product portfolio: From tower model to DLC rack model

- Tower 1VE
- Rackmount 4VE/1U
- Rackmount 8VE/4U
- DLC rackmount 8VE/4U
- High Density DLC rackmount 8VE/2U
- DLC Rack 64VE
- High Density DLC Rack 144VE
## VE roadmap

<table>
<thead>
<tr>
<th>Spec</th>
<th>VE10</th>
<th>VE10E</th>
<th>VE20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core/CPU</td>
<td>8</td>
<td>8</td>
<td>~10</td>
</tr>
<tr>
<td>Core performance</td>
<td>~307GF(DP)</td>
<td>~304GF(DP)</td>
<td>307GF (DP)</td>
</tr>
<tr>
<td></td>
<td>~614GF(SP)</td>
<td>~608GF(SP)</td>
<td>614GF (SP)</td>
</tr>
<tr>
<td>CPU performance</td>
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<td>~3.07TF (DP)</td>
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<tr>
<td></td>
<td>~4.91TF(SP)</td>
<td>~4.86TF(SP)</td>
<td>~6.14TF (SP)</td>
</tr>
<tr>
<td>Cache capacity</td>
<td>16MB shared</td>
<td>16MB shared</td>
<td>16MB shared</td>
</tr>
<tr>
<td>Memory Bandwidth</td>
<td>~1.22TB/s</td>
<td>~1.35TB/s</td>
<td>1.53TB/s</td>
</tr>
<tr>
<td>Memory capacity</td>
<td>24GB/48GB</td>
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<td>48GB</td>
</tr>
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Studies for the future VE
## VE roadmap

<table>
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<tr>
<th>Spec</th>
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<th>VE10E</th>
<th>VE20</th>
<th>VE30</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core/CPU</td>
<td>8</td>
<td>8</td>
<td>~10</td>
<td>???</td>
</tr>
<tr>
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<td>48GB</td>
<td>???</td>
</tr>
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</table>
VE20 Memory Subsystem

- **High bandwidth**
  - 409.6GB/s x2 core bandwidth
  - Over 3TB/s LLC bandwidth
  - 1.53TB/s memory bandwidth

- **Caches**
  - Scalar L1/L2 caches in each core
  - 16MB shared LLC

- **Two memory networks**
  - 2D mesh NoC for core memory access
  - Ring bus for DMA and PCIe traffic

- **DMA engine**
  - Used by both vector cores and x86 node
  - Can access VE memory, VE registers, and x86 memory
Approaches to memory subsystem design

- Bandwidth enhancement !!
  - Huge amount of wiring required to implement NoC

- Reduce required bandwidth
  - Partitioning
NUMA(Partitioning) mode

- VE software cares memory coherency of a user process between two domains.
  - ½ Installed cores
  - ½ LLC size
  - ½ Memory size

- Process management, memory management and commands are optimized for the HW mode.

- User can use the Partitioning mode like NUMA.
NUMA performance sample

NUMA friendly codes can have better performance

- HPCG: x1.18 performance growth compared to the normal (non-NUMA) mode
Approaches to memory subsystem design

Bandwidth enhancement !!!
- Huge amount of wiring required to implement NoC

Reduce required bandwidth
- Partitioning
- Add private cache for CORE
Performance simulation

Performance simulator

- It is possible to experiment by changing the amount of resources in CPU such as buffers existing in the pipeline.
- We made some code run for sample code A, B, C, D, E, F.

study

- Place a CORE private cache between CORE and NoC of the memory subsystem of VE and observe the performance.
## Results

<table>
<thead>
<tr>
<th>Program</th>
<th>Number of instructions</th>
<th>Instruction rate (Arith:LD:ST)</th>
<th>VL length (average)</th>
<th>CORE private cache hit ratio</th>
<th>GFlops growth (cache added/VE20)</th>
</tr>
</thead>
<tbody>
<tr>
<td>sample A</td>
<td>813k</td>
<td>0.998 :1: 0.002</td>
<td>255.5</td>
<td>47.0%</td>
<td>1.68</td>
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<tr>
<td>sample B</td>
<td>546k</td>
<td>1.110 :1: 0.769</td>
<td>171.8</td>
<td>5.2%</td>
<td>0.99</td>
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<tr>
<td>sample C</td>
<td>3426k</td>
<td>1.107 :1: 0.444</td>
<td>181.4</td>
<td>26.8%</td>
<td>1.22</td>
</tr>
<tr>
<td>sample D</td>
<td>345k</td>
<td>1.076 :1: 0.154</td>
<td>101</td>
<td>8.6%</td>
<td>1.03</td>
</tr>
<tr>
<td>sample E</td>
<td>402k</td>
<td>1.035 :1: 0.071</td>
<td>256</td>
<td>39.3%</td>
<td>1.24</td>
</tr>
<tr>
<td>sample F</td>
<td>68k</td>
<td>7.027 :1: 0.400</td>
<td>255.9</td>
<td>2.9%</td>
<td>0.97</td>
</tr>
</tbody>
</table>
How to improve VE30 performance?

We need to strengthen the memory subsystem.

There is a big challenge how to implement NoC.

Adding a private cache for CORE can be an effective option.
Find more information on our website

Aurora Forum Web
http://www.hpc.nec

- Latest updates
- Manual, documents
- Bulletin board

SX-Aurora TSUBASA Website

- Hardware and software overview
- Supported applications

https://jpn.nec.com/hpc/sxauroratsubasa/

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