Experiences with NEC’s New Vector System
SX-Aurora TSUBASA and Its Extension for the Future

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Today’s Agenda

★ Quick Introduction of NEC’s New Vector System: SX-Aurora TSUBASA
  ✓ An X86-Attached SX Vector System Aiming at Standardization and Customization
  ✓ The New Execution Model of Scalar/OS Offloading

★ Early Evaluation of SX-Aurora TSUBASA
  ✓ Tohoku Univ.’s Application Kernels
  ✓ HPCG
  ✓ Vector Offloading Mechanism

★ On-going R&D
  ✓ Design consideration of SX-Aurora TSUBASA for the Next Generation
  ✓ R&D of a Quantum Computing-Assisted HPC Infrastructure
The First Impression of SX-Aurora TSUBASA
NEC Brand-New Vector System: SX-Aurora-Tsubasa

Features

⭐ Customization
- Highest Mem. BW
- Largest Single Core Performance

⭐ Standardization
- Linux Environment
- New execution model centralized on vector computing

Source: NEC
Hardware Specification of SX-Aurora TSUBASA

SX Vector Processor

Vector Engine (VE) | Type 10B
---|---
Frequency | 1.4 GHz
Performance/Core | 537.6 GF(SP), 268.8 GF (DP)
No. of Cores | 8
Performance/Socket | 4.30 TFLOPS (SP) 2.15 TFLOPS (DP)
Memory Subsystem | HBM2 8GB x6
Memory Bandwidth | 1.2 TB/s
Memory Capacity | 48 GB

Vector Host (VH) | Intel Xeon Gold 6126
---|---
Frequency | 2.60 GHz / 3.70 GHz (Turbo boost)
Performance/Core | 166/236 GF(SP), 83/118 GF (DP)
No. of Cores | 12
Performance/Socket | 1,996/2,840 GF(SP) 998.4/1,420 GF(DP)
Memory Subsystem | DDR4-2666 DIMM 16GB x 6
Memory Bandwidth | 128 GB/s
Memory Capacity | 96 GB
A New Execution Model of SX-Aurora TSUBASA

Conventional Execution Model of Accelerators

- Host
  - PCIe Gen3
  - Start processing
  - Data transfers
  - Result transfer
  - Kernel execution
  - End processing
  - Data transfers easily become bottleneck

- GPU

SX-Aurora TSUBASA Execution Model

- VH
  - PCIe Gen3
  - Start processing
  - OS function
  - System calls (I/O, etc)
  - End processing

- VE
  - Start processing
  - System calls (I/O, etc)

Data transfer bottleneck among VH and VE can be avoided

Accelerator as a Slave!

Vector-Centric!
## Comparison between SX-ACE and SX-Aurora

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<tbody>
<tr>
<td>Number of Cores</td>
<td>8</td>
<td>4</td>
<td>2x</td>
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<tr>
<td>Total Flop/s in DP (Total Flop/sin SP)</td>
<td>2.15Tflop/s (4.3Tflop/s)</td>
<td>256Gflop/s</td>
<td>8.4x (16.8x)</td>
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<tr>
<td>Memory Bandwidth</td>
<td>1.2TB/sec</td>
<td>256GB/sec</td>
<td>4.7x</td>
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<tr>
<td>ADB Capacity</td>
<td>16MB(Shared)</td>
<td>4MB(Private)</td>
<td>16x</td>
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<td>B/F</td>
<td>0.55</td>
<td>1</td>
<td>0.55x</td>
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<tr>
<td>OS</td>
<td>Linux</td>
<td>Super-UX</td>
<td>无限</td>
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# Comparison between Xeon Gold, SX-Aurora TSUBASA VE and V100

<table>
<thead>
<tr>
<th></th>
<th>Intel Xeon Gold 6126</th>
<th>NEC Vector Engine Type 10B</th>
<th>NVIDIA Tesla V100</th>
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<tbody>
<tr>
<td><strong>Frequency</strong></td>
<td>2.6 GHz / 3.7 GHz (Turbo)</td>
<td>1.4 GHz</td>
<td>1.245 GHz</td>
</tr>
<tr>
<td><strong>No. of cores</strong></td>
<td>12</td>
<td>8</td>
<td>5120</td>
</tr>
<tr>
<td><strong>Performance/socket</strong></td>
<td>1,996/2,840 GF (SP) 998.4/1,420 GF (DP)</td>
<td>4.3 TF (SP) 2.15 TF (DP)</td>
<td>14 TF (SP) 7 TF (DP)</td>
</tr>
<tr>
<td><strong>Memory subsystem</strong></td>
<td>DDR4-2666 DIMM 16GB x 6 channels</td>
<td>HBM2 8GB x 6 modules</td>
<td>HBM2 4GB x 4 modules</td>
</tr>
<tr>
<td><strong>Memory bandwidth</strong></td>
<td>128 GB/s</td>
<td>1.22 TB/s</td>
<td>900 GB/s</td>
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<tr>
<td><strong>Memory capacity</strong></td>
<td>96 GB</td>
<td>48 GB</td>
<td>16 GB</td>
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<td><strong>Price?</strong></td>
<td>≃</td>
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</table>
You may be interested in Post-K Processor…
~Become available in 2021?~

**A64FX Chip Overview**

**Architecture Features**
- Armv8.2-A (AArch64 only)
- SVE 512-bit wide SIMD
- 48 computing cores + 4 assistant cores*
  *All the cores are identical
- HBM2 32GiB
- Tofu 6D Mesh/Torus
  28Gbps x 2 lanes x 10 ports
- PCIe Gen3 16 lanes

**7nm FinFET**
- 8,786M transistors
- 594 package signal pins

**Peak Performance (Efficiency)**
- >2.7TFLOPS (>90%@DGEMM)
- Memory B/W 1024GB/s (>80%@Stream Triad)

The Similar Architecture with The Same Performance Available Right Now!

Vector Engine Processor Overview

Components
- 8 vector cores
- 16MB LLC
- 2D mesh network on chip
- DMA engine
- 6 HBM2 controllers and interfaces
- PCI Express Gen3 x16 interface

Specs

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
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<tbody>
<tr>
<td>Core frequency</td>
<td>1.6GHz</td>
</tr>
<tr>
<td>Core performance</td>
<td>307GF(DP)</td>
</tr>
<tr>
<td></td>
<td>614GF(SP)</td>
</tr>
<tr>
<td>CPU performance</td>
<td>2.45TF(DP)</td>
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<tr>
<td></td>
<td>4.91TF(SP)</td>
</tr>
<tr>
<td>Memory bandwidth</td>
<td>1.2TB/s</td>
</tr>
<tr>
<td>Memory capacity</td>
<td>24/48GB</td>
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</tbody>
</table>

Technology
- 16nm FinFET process
- 4.8 billion transistors

## Benchmark Programs for Performance Evaluation

<table>
<thead>
<tr>
<th>Kernels</th>
<th>Fields</th>
<th>Methods</th>
<th>Memory access</th>
<th>Grids</th>
<th>Code B/F</th>
<th>Vector Length</th>
<th>Vector Ratio</th>
<th>Actual B/F</th>
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</thead>
<tbody>
<tr>
<td>Land Mine</td>
<td>Electromagnetic</td>
<td>FDTD</td>
<td>Sequential</td>
<td>100x750x750</td>
<td>6.22</td>
<td>250.9</td>
<td>99.2</td>
<td>5.14</td>
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<tr>
<td>Earthquake</td>
<td>Seismology</td>
<td>Dependent Friction Law</td>
<td>Sequential</td>
<td>2047x2047x256</td>
<td>4.00</td>
<td>255.9</td>
<td>99.4</td>
<td>4.00</td>
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<tr>
<td>Turbulent Flow</td>
<td>CFD</td>
<td>Navier-Stokes</td>
<td>Sequential</td>
<td>512x16384x512</td>
<td>8.00</td>
<td>255.8</td>
<td>99.1</td>
<td>1.47</td>
</tr>
<tr>
<td>Antenna</td>
<td>Electromagnetic</td>
<td>FDTD</td>
<td>Sequential</td>
<td>252755x9x97336</td>
<td>1.73</td>
<td>255.7</td>
<td>99.7</td>
<td>0.98</td>
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<tr>
<td>Plasma</td>
<td>Physics</td>
<td>Lax-Wendroff</td>
<td>Indirect</td>
<td>20M</td>
<td>0.82</td>
<td>256.0</td>
<td>70.9</td>
<td>0.11</td>
</tr>
<tr>
<td>Turbine</td>
<td>CFD</td>
<td>LU-SGS</td>
<td>Indirect</td>
<td>480x80x80x10</td>
<td>0.96</td>
<td>239.5</td>
<td>99.7</td>
<td>0.0084</td>
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Tohoku Univ.’s Kernels Results

<table>
<thead>
<tr>
<th></th>
<th>SX-Aurora TSUBASA</th>
<th>SX-ACE</th>
<th>Skylake</th>
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<tbody>
<tr>
<td>Land mine</td>
<td>4.2X</td>
<td>0.4X</td>
<td>0.5X</td>
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<tr>
<td>Earthquake</td>
<td>2.9X</td>
<td>0.5X</td>
<td>0.7X</td>
</tr>
<tr>
<td>Turbulent flow</td>
<td>3.4X</td>
<td>1.4X</td>
<td>1.4X</td>
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<tr>
<td>Antenna</td>
<td>9.7X</td>
<td>2.0X</td>
<td>0.5X</td>
</tr>
<tr>
<td>Plasma</td>
<td>3.5X</td>
<td>0.6X</td>
<td>0.6X</td>
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<thead>
<tr>
<th></th>
<th>C B/F</th>
<th>S B/F</th>
<th>Vec. Length</th>
<th>Vectrization</th>
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<tr>
<td>Land mine</td>
<td>6.22</td>
<td>5.14</td>
<td>250.9</td>
<td>99.21</td>
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<tr>
<td>Earthquake</td>
<td>4.00</td>
<td>4.00</td>
<td>255.9</td>
<td>99.38</td>
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<tr>
<td>Turbulent flow</td>
<td>8.00</td>
<td>1.47</td>
<td>255.8</td>
<td>99.07</td>
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<tr>
<td>Antenna</td>
<td>1.73</td>
<td>0.98</td>
<td>255.7</td>
<td>99.74</td>
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<tr>
<td>Plasma</td>
<td>0.82</td>
<td>0.11</td>
<td>255.9</td>
<td>70.94</td>
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<tr>
<td>Turbine</td>
<td>0.96</td>
<td>0.0084</td>
<td>239.5</td>
<td>99.71</td>
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Performance Evaluation of SX-Aurora TSUBASA by Using the HPCG Benchmark

★ HPCG (High Performance Conjugate Gradients) is designed to exercise computational and data access patterns that more closely match a broad set of important applications,

✓ HPL for top500 is increasingly unreliable as a true measure of system performance for a growing collection of important science and engineering applications.

★ HPCG is a complete, stand-alone code that measures the performance of basic operations in a unified code:

✓ Sparse matrix-vector multiplication.
✓ Sparse triangular solve.
✓ Vector updates.
✓ Global dot products.
✓ Local symmetric Gauss-Seidel smoother.
✓ Driven by multigrid preconditioned conjugate gradient algorithm that exercises the key kernels on a nested set of coarse grids.
✓ Reference implementation is written in C++ with MPI and OpenMP support.

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Kernel</th>
<th>Required B/F</th>
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<tbody>
<tr>
<td>HPL</td>
<td>DGEMM</td>
<td>&lt; 0.1</td>
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<td>HPGMG</td>
<td>GSRB</td>
<td>&gt; 1</td>
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<tr>
<td>HPCG</td>
<td>SpMV, SYMGS</td>
<td>&gt;4</td>
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</table>
Sustained Performance of HPCG-Benchmark

HPCG result (Gflop/s)

Grid sizes

SX-Aurora TSUBASA

SX-ACE

2.34x
HPCG-Benchmark Efficiency

Efficiency (%) vs Grid sizes

- SX-Aurora TSUBASA
- SX-ACE

System | Eff. (%)  
--- | ---  
SX-ACE | 10.8  
K/FX | 3.7  
Xeon | 2.2  
BlueGene | 1.5  
GPU | 1.4  
XeonPhi | 1.0  
Sunway TaihuLight | 0.3  

Hiroaki Kobayashi, Tohoku University
Evaluation of the New Execution Model: OS/Scalar Offloading from Vector Processing

Offloading of OS and scalar operations

VH Offloading Mode

Offloading of vector operations

VE Offloading Mode

VH Offloading

VE Offloading

Oct. 9-10, 2018
Impressions of SX-Aurora TSUBASA

🌟 SX-Aurora TSUBASA has a great potential to achieve a high sustained performance for memory-intensive applications, but…

✔ Compiler development is still underway, limiting the sustained performance regarding auto-vectorization and auto-parallelization, anyway use the latest one for the best performance!

✔ Compiler is also not fully exploiting enlarged and core-shared capacity of LLC. Software controlled function is desired to make the best use of it for reducing off-chip memory transactions.

✔ For some applications, the LLC bandwidth to cores becomes a bottleneck even with a high hight rates.

 обраща́ется в ходе сеанса общения с ассистентом в области науки и техники.
Unofficial Web Site of SX-Aurora TSUBASA

http://www.cal.is.tohoku.ac.jp/_wp/en/2018/06/15/how-to-install-sx-aurora-tsubasa/

- Our website provides the information about
  - How to setup software environments
  - How to update software environments
  - Events
  - etc
Design Consideration of the Future Vector Systems *

*This work is partially conducted with NEC, but the contents do not reflect any future products of NEC.*
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<tr>
<td>Systems &amp; Facility</td>
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<td>SX-9 (29TF)</td>
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<td>New HPC Building Construction (1,500m²)</td>
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<td>5-Cluster SX-ACE (707TF)</td>
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<td>Storage Systems (4PB)</td>
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<td>3D Tiled Display</td>
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<td>Design and Procurement process for enhancement of Server, Storage &amp; Visualization Systems</td>
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<td>Design and Procurement process of the next supercomputer system</td>
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<td>Feasibility study for future HPC</td>
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<td>Next System??</td>
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Timeline of the Cyberscience Center HPC System Development and R&D For the Future
Reenforce the academic and industry collaboration for the HPC R&D at Tohoku University

★ Tohoku-Univ NEC Joint Research Division of High-Performance Computing
★ Founded in June, 2014, 8-Year Period until 2022

★ Objectives

- R&D on HPC technologies to exploit high-sustained performance of science and engineering applications on current HPC Systems and to realize Future HPC Systems targeting at 2021
- Evaluation and Improvement of the current HPC environments through migration of SX-9 applications to SX-ACE
- Detailed Evaluation and Analysis of Modern HPC Systems, not only Vector Systems but also Scalar-Parallel and Accelerator-Based Systems
- Feasibility study of a future highly balanced HPC system for high sustained performance of practical applications in the post-peta scale era

★ Faculty Members

- Hiroaki Kobayashi, Professor and division director
- Hiroyuki Takizawa, Professor
- Ryusuke Egawa, Associate Professor
- Akihiko Musa (NEC), Visiting Professor
- Mitsuo Yokokawa (Kobe Univ), Visiting Professor
- Shintaro Momose (NEC), Visiting Associate Professor
- Masayuki Sato, Assistant Professor
- In collaboration with visiting researchers from NEC and the technical staff of Cyberscience Center
Scaling may be End, but Silicon is not End! And Use it Smart and Effective!

- We are facing the end of Moore’s law due to the physical limitations, and the transistor cost is hard to reduce, however.
- Silicon is still fundamental constructing material for computing platforms such as plastic, steel and concrete for automobiles, buildings and home appliances.

⭐ So, we have to become much more smart for design of Future HEC systems.
⭐ Use precious silicon budget (+ advanced device technologies) to effectively design mechanisms that can maximize the sustained performance and power-efficiency of individual applications domains.

It’s time to focus on Domain-Specific Architectures (DSAs) for computation-intensive, memory-intensive, I/O intensive, low-precision computing... etc applications to improve silicon/power efficiency!

New HPC System Architecture Design Concept of Ensemble Architecture:
Make different DSAs combine and complementary work together to realize the general-purpose functionality as a single computing infrastructure
Domain Specific Balanced Architecture Design Approach: Not Peak Performance, Turn Memory-BW into Sustained Performance!

Need balanced improvement both in flop/s and BW! for high-efficiency in wide application areas

For computation-intensive applications only!

Our target: High B/F oriented design

Flop/s-oriented, memory-limited design
What Does the Next Vector System Look Like in Year Around 2020-2021?

★★Vector Engine Spec.
- The 7nm Technology becomes available?
- 5X more transistors from 16nm tech?
- 5X in # of Cores, i.e. 50 VE cores feasible?
- up to 15TF, if the core performance is same, but should be lowered due to power/thermal limitation of the chip.

★★Memory Subsystem
- 2x in Memory BW, and 1.5X in Memory Capacity when using HBM 3 under the assumption of the same chip size of Aurora-TSUBASA
- ~3TB/s and ~96GB??

★★Design targets of 0.5BF (20 cores of 6TF for memory-intensive applications) to 0.25 BF (40 Cores of 12TF for compute-intensive applications)
- be competitive with contemporary HEC systems at that time, such as Post-K (JP), A21 (US), NERSC-9 (USA), Crossroads (US), EU Exa-System (FR/GE), NUDT2020 (Ch)…
What Does the Next Vector System Look Like in Year Around 2020-2021? (Cont’d)

★ How 20~40 cores are integrated and connected.

- Single chip or multi-chip (SIP)?
- If SIP is employed, how multiple chips are connected?
  ≡ If EMIB available, BW could be increased?
  ≡ Silicon photonics with WDM becomes available?
- Single SMP or clustered SMP
- Crossbar, mesh, ring, etc or their hierarchical and hybrid?
- Coherency protocol of ADB (Snoopy or Directory)

32 Cores, 9.6TF, 3TB/s, 0.3BF

Source by IBM

Source by Intel
Quantum Computer: Emerging Domain Specific Architecture

★ Quantum computing is drawing much attention recently as an emerging technology in the era of post-Moore

✔ In particular, quantum computers for quantum annealing are commercialized by the D-wave systems, and their applications are developed world-wide.

✔ Google, NASA, Volkswagen, Lockheed, Denso…

✔ The base model named the Ising model to design and implement the D-wave machines has been proposed by Prof. Nishimori et al of Tokyo Inst. Tech. In 1998.

★ The quantum annealing is a metaheuristic for finding the global minimum of a given objective function over a given set of candidate solutions (candidate states), by a process using quantum fluctuations

An ideal solver for combinatorial problems!
Toward Realization of Quantum Computing-Assisted HPC Infrastructure

★ Tohoku University has established an interdisciplinary priority research institute, named Q-HPC, for Quantum Computing-Accelerated HPC in 2018

★ As Q-HPC members, we start a new 5-year research program named “R&D of Quantum Annealing-Assisted HPC Infrastructure”, supported by MEXT

✓ Becomes an innovative infrastructure to develop next-generation applications in the fields of computational science, data sciences and their fusions

✓ Provides transparent accesses to not only classical HPC resources but also Quantum Computing one in a unified fashion.

Innovative Applications in the fields of Computational Science, Data Science and their Fusion

QA-Assisted HPC infrastructure

Inductive Processing (for Data Science)  Coupling  Deductive Processing (for Computational Science)

QA Platform

QA-Assisted AI•ML Platform

D-Wave Machines

X86-Assisted Vector Computing Platform

SX-Aurora TSUBASA and its Successors
Team Organization

- Architecture/System Software Gr
- AI•Machine Learning Gr
- Application Gr
- Quantum Annealing Gr

Digital Twin Numerical Turbine
Prof. Satoru Yamamoto et al. (Tohoku Univ.)

Real-Time Tsunami Inundation Damage Analysis and Optimal Evacuation Planning
Prof. Shun-ichi Koshimura et al. (Tohoku Univ.)

System Software:
Profs. Hiroyuki Takizawa, Ryusuke Egawa et al. (Tohoku Univ.)
Akihiro Musa et al. (NEC)

Inductive Processing
Prof. Kazuhiko Komatsu (Tohoku Univ.)
Takashi Hagiwara et al. (NEC)
Prof. Masayuki Ozeki et al. (Tohoku Univ.)

Deductive Processing
Architecture
Prof. Hiroaki Kobayashi et al. (Tohoku Univ.)
Prof. Mitsuo Yokokawa (Kobe Univ.)
Shintaro Momose Shigeyuki Aino et al. (NEC)

International Advisory Committee:
Mateo Valero (BSC,ES) Michael Resch (HLRS,DE), Vladimir Voevodin (MSU,RU),
Bo Ewald(D-wave, CA), Hans Peter Graf (NEC Lab. America, US)
An Example of Target Application:
QA-Enhanced Real-Time Tsunami Inundation Forecasting and Optimal Evacuation Planning

Fault Estimation with MCMC

Tsunami Inundation Simulation

Optimal Evacuation Planning with Quantum Annealing

Integrated Programming Framework

D-wave Machine

Aurora TSUBASA Vector Host (Xeon)

Aurora TSUBASA Vector Engine

Cyberscience Center

Graduate School of Information Sciences, Tohoku University
An Example of Target Applications: Digital Twin Numerical Turbine

Cyber Data

Numeric Turbine as Digital Twin

Estimation of internal situation of real systems

Simulation Database

AI·Machine Learning

Observed Data from the Real-System

Simulations based on many Scenarios

Real System

Physical Data
Let’s Meet together again at the next WSSP at Tohoku Univ.

⭐ 29th Workshop on Sustained Simulation Performance

- Date: March 19-20, 2019
- Place: Tohoku University