Accelerators – Trends & Ideas

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Springer Book „Sustained Simulation Performance 2016“

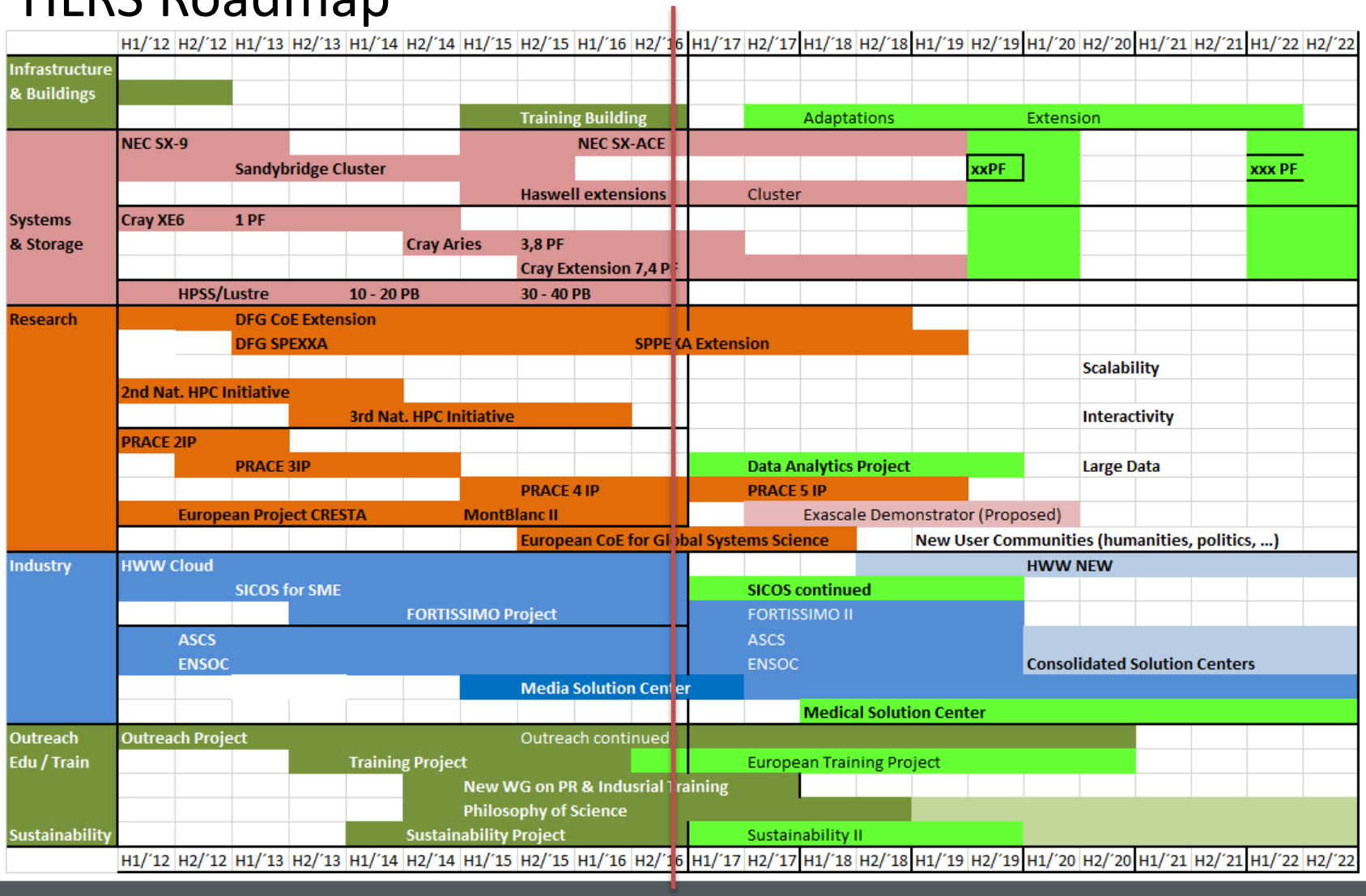
- Dear Editors,
- We are very pleased to inform you that your book has been published and it is available on http://link.springer.com/book/10.1007/978-3-319-46735-1.
- Customers can order it via http://www.springer.com/in/book/9783319467344#.

Outline

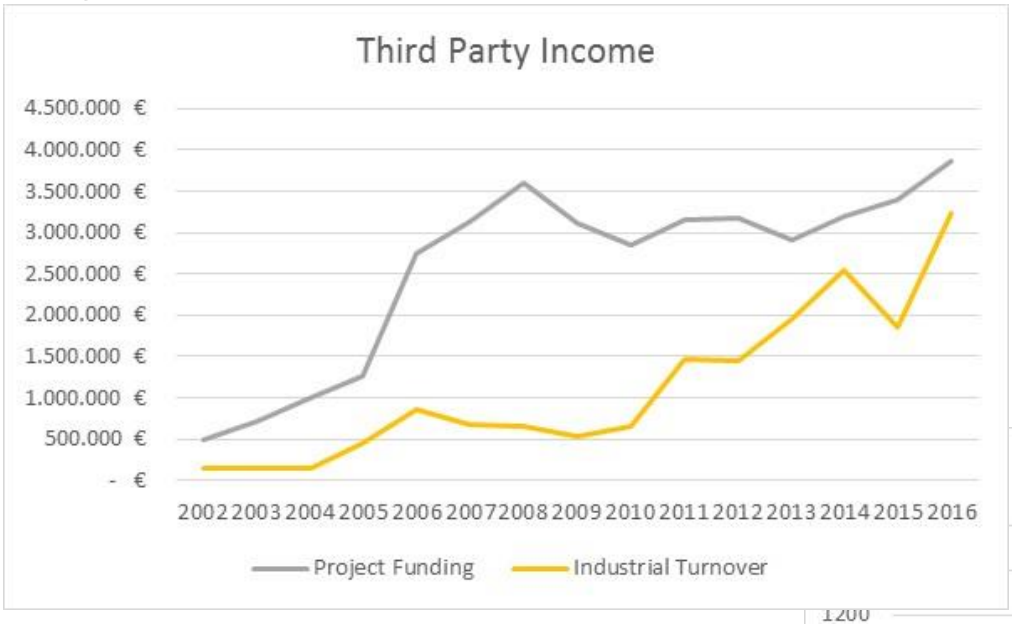
- A few words about HLRS
- A few words about accelerators
- Conclusions

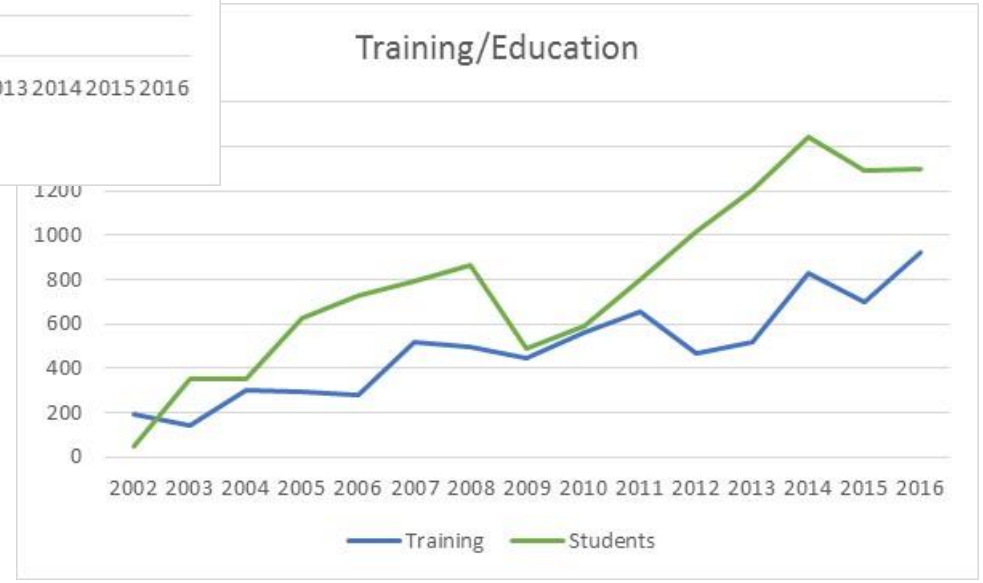
HLRS

HLRS Roadmap



Key Performance Indicators





ACCELERATORS

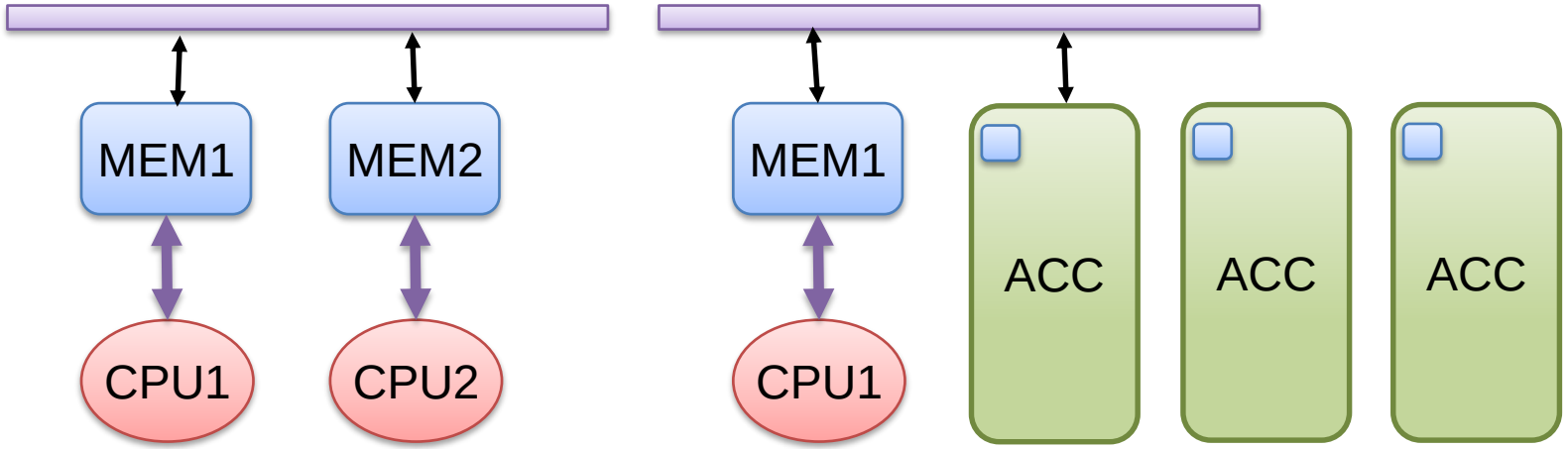
Accelerators in the TOP500

Name	Computer	Total Cores
Sunway TaihuLight	Sunway MPP, Sunway SW26010 260C 1.45GHz, Sunway	10649600
Tianhe-2 (MilkyWay-2)	TH-IVB-FEP Cluster, Intel Xeon E5-2692 12C 2.200GHz, TH Express-2, Intel Xeon Phi 31S1P	3120000
Titan	Cray XK7 , Opteron 6274 16C 2.200GHz, Cray Gemini interconnect, NVIDIA K20x	560640
Sequoia	BlueGene/Q, Power BQC 16C 1.60 GHz, Custom	1572864
Cori	Cray XC40, Intel Xeon Phi 7250 68C 1.4GHz, Aries interconnect	622336
Oakforest-PACS	PRIMERGY CX1640 M1, Intel Xeon Phi 7250 68C 1.4GHz, Intel Omni-Path	556104
K Computer	SPARC64 VIIIfx 2.0GHz, Tofu interconnect	705024
Piz Daint	Cray XC50, Xeon E5-2690v3 12C 2.6GHz, Aries interconnect , NVIDIA Tesla P100	206720
Mira	BlueGene/Q, Power BQC 16C 1.60GHz, Custom	786432
Trinity	Cray XC40, Xeon E5-2698v3 16C 2.3GHz, Aries interconnect	301056

Theoretical Advantages

- SIMD style architecture
- Higher number of cores
- Higher peak performance
- Higher potential for future improvement
- Not only made by Intel
- Easy to plug in (even into your local workstation)

Architectures (schematic)



Traditional Node

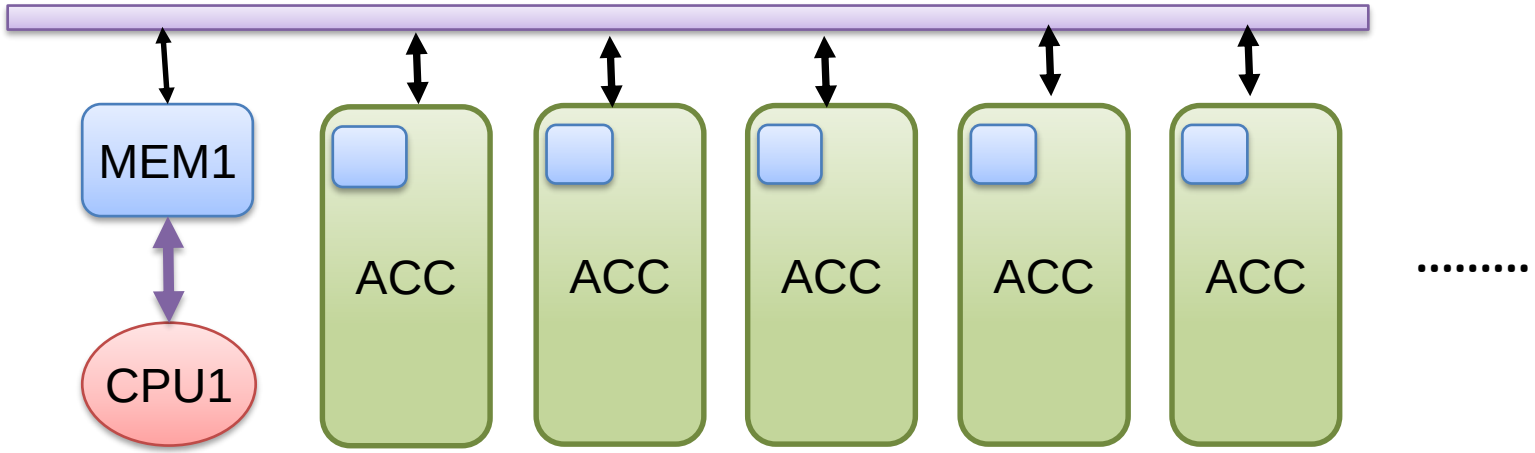
Standard Node using Accelerators

Practical Challenges

- Slow connection to memory
- Small local memory
- Non-standard programming

My favorite accelerator concept

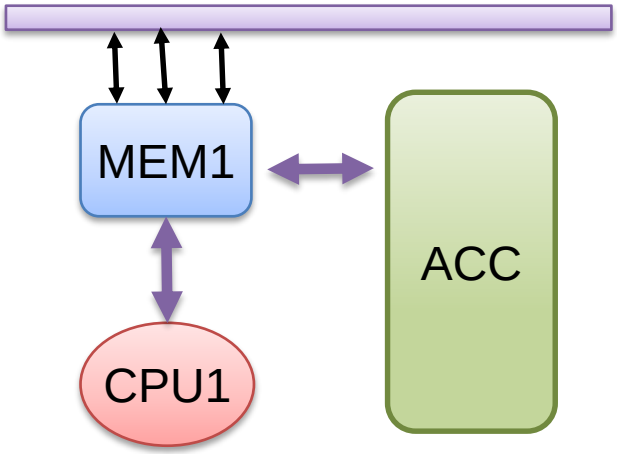
What we can expect to see



- Somewhat faster path to memory
- Somewhat bigger local memory
- Non-standard programming

An option for a compromise

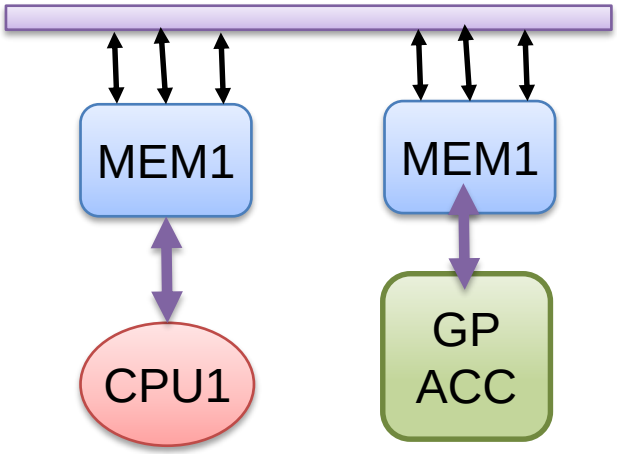
Hybrid node using an accelerator that can access the same memory



- **Less slow** connection to memory
- **Big** memory
- **Non-standard programming (there are ways to overcome this)**

Another option for a compromise

Hybrid node using a general purpose accelerator that has its own big/fast memory



- **Fast** connection to memory
- **Big** memory
- **Standard programming**

CONCLUSIONS

My 5 cent

- Architectures are driven by accelerator technology
- There is limited hope for accelerators that can solve real world engineering problems easily
- There is ample room for better solutions
- The laws of the market suggest that someone will fill this niche

Questions