HLRS Workshop

Monday 28th October – Thursday 31st October, 2013

The 4 day workshop will give attendees the knowledge required to understand the most optimal way to port, optimize and execute applications on the HLRS Cray XE/XC service. The workshop is a mixture of lectures and practical sessions. Example exercises will be provided but attendees are encouraged to bring along their own applications to the workshop. Although specifically targeting the Cray architecture and programming environment much of the lessons learned with be more generally useful.

The first three days, specialists from Cray will support you in your effort porting and optimizing your application on our Cray XE6. The Cray presenters are Stefan Andersson, Aniello Esposito, Michael Neff, and Stephen Sachs from HLRS on-site application support team and Cray Computer Deutschland GmbH. On the fourth day, Georg Hager and Jan Treibig from RRZE will present detailed information on optimizing codes on the multicore AMD Interlagos and Intel Sandy Bridge processors.

First Day

Attendees will learn about the Cray XE/XC architecture and its programming environment and gain a basic overview of scientific libraries. They will have an initial understanding of how to port their applications to the XC30/XE6 platforms at HLRS and have an opportunity to work on the port in dedicated sessions under the supervision of the Cray staff. A short introduction to debugging tools on the Cray platforms should help to resolve failures of the initial port.

09:00 – 09:30 Registration		
09:30 – 10:00 Welcome	HLRS/Cray	Page
10:00 – 10:45 Overview of the Cray XE/XC Architecture	Stephen Sachs	2
10:45 – 11:15 Programming Environment for the Cray system	Stephen Sachs	18
11:15 – 11:45 Cray Scientific Libraries I	Stephen Sachs	24
11:45 – 12:00 Break		
12.00 – 12:45 Compiling and running Applications	Aniello Esposito	29
12:45 – 13:00 Introduction to the Hands-on Exercises	Aniello Esposito	---
13:00 – 14:00 Lunch		
14:00 – 15:00 Hands-on: Porting Applications	Cray/attendees	
15:00 – 15:30 Introduction to Debugging Tools	Aniello Esposito	39
15:30 – 15:45 Break		
15:45 – 16:45 Hands-on: Porting Applications	Cray/attendees	
16:45 – 17:15 Q&A, Round-Table on first Experiences	Cray/attendees	

Evening Social Event: guided city tour and dinner (self-paying)

Second Day

The attendees will have an initial understanding of how to identify performance bottlenecks of scientific applications and potential causes using the Cray Performance tools. They will use CrayPat, Cray Reveal and Cray Apprentice2 for profiling and visualization and in addition there will be a live demonstration of Reveal. During hands on labs the attendees will have the opportunity to tune their applications under the supervision of Cray staff. Load imbalance, rank placement, and MPI tuning via environment variables will be discussed in the afternoon.

09:00 – 09:45 Introduction to Performance Analysis	Michael Neff	46
09:45 – 10:45 Hands-on: Analyzing Applications	Cray/attendees	
10:45 – 11:00 Break		
11:00 – 11:30 Performance Analysis (Single core/socket/node)	Michael Neff	57
11:30 – 12:00 Reveal Demo	Aniello Esposito	---
12:00 – 13:00 Hands-on: Analyzing Applications	Cray/attendees	
13:00 – 14:00 Lunch		
14:00 – 14:30 MPI Environment Variables	Stephen Sachs	65
14:30 – 15:30 Hands-on: Tuning Applications	Cray/attendees	
15:30 – 15:45 Break		
15:45 – 16:15 Load Imbalance & Rank Placement	Stephen Sachs	74
16:15 – 17:00 Hands-on: Tuning Applications	Cray/attendees	
17:00 – 17:30 Q&A, Round-Table on first Experiences	Cray/attendees	

Third Day

The attendees will learn various optimization techniques related to single CPUs and Input/Output. In the hands on lab they will continue to tune their applications. The afternoon is dedicated to an overview of MPI3 and PGAS and a short overview of Coarray Fortran and Unified Parallel C.

Fourth Day

The fourth day is dedicated to single-core and single-node performance and optimization in the multi-core and multi-socket environment with the Interlagos and Sandy Bridge CPUs in Cray XE6/XC30 systems. After introducing the basic architectural features we demonstrate simple performance modeling techniques, so that attendees get a clear view on the typical bottlenecks and performance patterns that are present on multicore nodes.

09:00 – 10:15 Lectures and hands-on
10:15 – 10:30 Break
10:30 – 11:45 Lectures and hands-on
11:45 – 12:00 Break
12:00 – 13:00 Lectures and hands-on
13:00 – 14:00 Lunch
14:00 – 15:00 Lectures and hands-on
15:00 – 15:15 Break
15:15 – 16:30 Lectures and hands-on

- **Introduction**
  - Architecture of multisocket multicore systems, with a special focus on the Interlagos and Sandy Bridge chips in Cray XE/XC
  - Node topology: cores, caches, chips, ccNUMA
  - Core architecture and typical bottlenecks
  - Data parallelism: SIMD and its implications
  - Data transfer through the cache hierarchy
  - Performance composition
- **Multicore performance and tools**
  - Affinity enforcement
  - Performance counter measurements
  - Basics and best practices for performance counter profiling
- **Microbenchmarking for architectural exploration**
- **Roadblocks for scalability on multicore chips**
  - Scaling properties and typical OpenMP overhead
  - Bandwidth saturation in cache and main memory
- **Optimal utilization of parallel resources**
  - Programming for SIMD parallelism
  - Programming in ccNUMA environments
- **Simple performance modeling: The Roofline Model**
  - Introduction to the Roofline Model
  - Example: “Simple” streaming loops
  - Example: Understanding and optimizing the performance of a Jacobi stencil code
  - Example: Sparse matrix-vector multiplication
  - Outlook: Extending the roofline model

Literature:
Georg Hager and Gerhard Wellein: Introduction to High Performance Computing for Scientists and Engineers. Chapman & Hall / CRC Press, 2010, 356 pages. ISBN 978-1-4398-1192-4.