First Day

Attendees will learn about the Cray XE architecture and its programming environment. They will have an initial understanding of potential causes of application performance bottlenecks, and how to identify some of these bottlenecks using the Cray Performance tools. The Attendees will use the Cray performance tools to profile their application.

09:00 – 09:30 Registration
09:30 – 09:40 Welcome
09:40 – 10:30 Overview of the Cray XE Architecture
- Short Cray onsite people introduction
- Node architecture
- Interconnect
- Processor architecture
- HLRS Setup
  - Pflops system
  - esLogin nodes, Visualization Server
  - IO setup

10:30 – 10:45 Break
10:45 – 11:30 Cray Linux Environment Review
- Overview
- CLE features
- Job launching & running a batch application
  - Interlagos specifics

11:30 – 11:45 Break
11:45 – 13:00 Programming Environment for the Cray XE system
- Overview
- Modules
- Compilers

13:00 – 14:00 Lunch
14:00 – 15:00 Performance measurement on the Cray XT system
- Overview
- Automatic Profiling Analysis
- Using Hardware Performance Counters
- Profile visualization with Cray Apprentice2

15:00 – 15:15 Break
15:15 – 15:30 Porting Applications: Best Practices
- Modules, includes, X64_32 error, …

15:30 – 17:30 Hands on Lab Profiling Applications

Second Day

We will finalize the presentations on how to identify performance bottlenecks. The attendees will use Cray Apprentice2 for performance visualization and will learn various optimization techniques. The attendees will start to tune their applications at the hands on lab.

09:00 – 10:30 Optimization Techniques I
- Memory hierarchy (TLB & cache)
- Tuning for Interlagos
- Communication
- Load imbalance

10:30 – 10:45 Break

10:45 – 12:00 Performance Analysis and Visualization I
- Performance analysis of MPI applications
- Performance Analysis of OpenMP Applications
- Load Imbalance Analysis
  - MPI Sync Time
  - Imbalance metrics
  - MPI Rank reorder

12:00 – 13:00 Optimization Techniques II, part 1
- MPI Optimization
  - Pre-posting receives
  - Task placement
- Huge Pages

13:00 – 14:00 Lunch

14:00 – 14:30 Optimization Techniques II, part 2

14:30 – 17:30 Hands on Lab Tuning applications

15:00 – Coffee and beverage available

Third Day

The attendees will learn advanced techniques to deal with scaling problems and how to access the on-line documentation for user help. In the hands on lab the attendees will continue to tune their applications.

09:00 – 10:00 I/O Optimization
- Using lustre
- Basic optimization
- MPI-IO

10:00 – 10:30 Performance Analysis and Visualization II
- Using Craypat for obtaining Memory statistics
- Trace analysis
  - Trace file generation
  - Trace visualization
- Performance tools user help
  - Using man pages
  - Using pat_help
  - Using Cray Apprentice2 on-line documentation

10:30 – 10:45 Break

10:45 – 11:30 Cray Debugger Support Tools
- Fast Track Debugging
- Stack Trace Analysis Tool (STAT)
- Abnormal Termination Processing

11:30 – 13:00 Cray Scientific and Math Libraries

13:00 – 14:00 Lunch

14:00 – 17:30 Hands on Lab Tuning applications

15:00 – Coffee and beverage available

Fourth Day

The fourth day is dedicated to single core performance and optimization in the multi-core and multi-socket environment with the Interlagos CPUs in Cray XE6 systems, together with scaling aspects of the communication in such hierarchical system architecture.

09:00 – 10:15 Lectures and hands-on
10:15 – 10:30 Break
10:30 – 11:45 Lectures and hands-on
11:45 – 12:00 Break
12:00 – 13:00 Lectures and hands-on
13:00 – 14:00 Lunch
14:00 – 15:00 Lectures and hands-on
15:00 – 15:15 Break
15:15 – 16:30 Lectures and hands-on

- **Introduction**
  - Architecture of multisocket multicore systems, with a special focus on AMD and Cray
  - Nomenclature
  - Current developments
  - SIMD and its implications
  - Programming models
- **Multicore performance and tools**
  - Scaling baselines
  - Affinity enforcement
  - Performance counter measurements
  - Basics and best practices for performance counter profiling
  - Examples
- **Impact of processor/node topology on performance**
  - General remarks on the performance properties of multicore/multisocket nodes
  - Bandwidth saturation effects
  - Simple performance modeling
    - OpenMP sparse MVM as an example for bandwidth-bound code
  - Programming for ccNUMA
  - OpenMP-specific performance issues
  - Shared resources on the core
  - Intranode vs. internode MPI

Days 1-3 are presented by Cray trainers, the forth day is taught by Georg Hager and Jan Treibig from RRZE. Literature:

> Georg Hager and Gerhard Wellein: Introduction to High Performance Computing for Scientists and Engineers. Chapman & Hall / CRC Press, 2010, 356 pages. ISBN 978-1-4398-1192-4.