Cray XE6 Optimization Workshop at HLRS, 2011, Feb. 2-4

Day 1: Basic Understanding of the Cray XE6

Registration
Welcome (Stefan Wesner, HLRS)
Cray XE6 Architecture (Stefan Andersson, Cray)
Architecture of Cray XE6
Socket 34 architecture
Gemini Interconnect
Break
The CRAY Programming Environment – Part I (Charles Henriet, Cray)
Modules
Compiler options and flags
Break
The CRAY Programming Environment – Part II (Charles Henriet, Cray)
Programming considerations
Running an application
Cray Scientific Libraries
Lunch
Optimization I
Optimization methodology (Jason J. Beech-Brandt, Cray)
Using Craypat to profile applications (Stefan Andersson, Cray)
Break
Hands-on workshop to profile applications
Compilation, Execution and profiling of applications on the CRAY XE6.
Attendees are encouraged having an application to work with

Day 2: Optimization and usage of the Cray XE6

9:00 – 10:30	Optimization II (Stefan Andersson, Cray)
	Memory understanding and optimization
	Vectorization
	Cache blocking examples
10:30 - 10:45	Break
10:45 – 12:00	Optimization III (Stefan Andersson, Cray)
	Shared Memory Optimization, Using OpenMP efficiently
	Using Craypat for examining OpenMP performance
12:00 – 12:45	Hands-on with Craypat
12:45 – 13:45	Lunch
13:45 – 15:15	Optimization IV (Stefan Andersson, Cray)
	Optimization of I/O
15:15 – 15:30	Break
15:30 – 17:30	Hands-on workshop to optimize applications

Day 3: Even more optimizations

9:00 - 10:30	Optimization V (Jason J. Beech-Brandt, Cray)
	Scaling applications to thousands of processors
	MPI optimization
	Task placement
10:30 - 10:45	Break
10:45 – 12:45	Co-array FORTRAN and UPC on Cray XE6 (Jason J. Beech-Brandt, Cray)
	Advantages and Disadvantages of MPI and PGAS
12:45 – 13:45	Lunch
13:45 – 15:15	Open Session for questions/review
15:15 – 15:30	Break
15:30 – 16:30	Hands on Workshop to optimize applications